IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets; comprising:

providing a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline;

designing a core cell having ~~a bitline~~ bitlines and ~~a~~ complementary bitlines ~~bitline~~;

designing a flipped core cell that has ~~a~~ flipped ~~bitline~~ bitlines and ~~a~~ flipped complementary ~~bitline~~ bitlines; and

arranging the core cell followed by the flipped ~~six transistor~~ core cell along each of the multiple pairs of the global ~~bitline~~ bitlines and the global complementary ~~bitline~~ bitlines.

2. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the ~~bitline~~ bitlines of the core cell is coupled with the flipped complementary ~~bitline~~ bitlines of the flipped core cell, and the complementary ~~bitline~~ bitlines of the core cell is coupled to the flipped ~~bitline~~ bitlines of the flipped core cell.

3. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 2, further comprising:

coupling successive pairs of the core cell and the flipped core cell along each of the multiple pairs of the global bitline and the global complementary bitline.

4. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the designing of the flipped core cell includes:

flipping the core cell horizontally about a Y-axis that is defined at a rightmost edge of the core cell to produce an intermediately flipped core cell; and

flipping the intermediately flipped core cell vertically about an X-axis that is defined at a lowermost edge of the intermediately flipped core cell to produce the flipped core cell.

5. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 4, wherein the ~~bitline~~ bitlines of the core cell is coupled with the flipped complementary ~~bitline~~ bitlines of the flipped core cell, and the complementary ~~bitline~~ bitlines of the core cell is coupled to the flipped ~~bitline~~ bitlines of the flipped core cell.

6. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 5, further comprising:

coupling successive pairs of the core cell and the flipped core cell along each of the multiple pairs of the global bitline and the global complementary bitline.

7. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 2, wherein the ~~bitline has~~ bitlines have a first capacitance and the complementary ~~bitline has~~ bitlines have a second capacitance.

8. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 7, wherein the flipped ~~bitline~~ bitlines have the first capacitance and the flipped complementary ~~bitline has~~ bitlines have the second capacitance.

9. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 8, further comprising:

achieving an equal capacitance on the global bitlines and the global complementary bitlines when the ~~bitline~~ bitlines of the core cell ~~is~~ are coupled with the flipped complementary ~~bitline~~ bitlines of the flipped core cell, and the complementary ~~bitline~~ bitlines of the core cell ~~is~~ are coupled to the flipped ~~bitline~~ bitlines of the flipped core cell.

10. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the memory device is fabricated onto a semiconductor chip.

11. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the memory device is designed using a memory generator.

12. (currently amended) A method of designing a memory device that has reduced bitline capacitance offsets ~~ina~~ in a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline, comprising:

providing a core cell having ~~a bitline~~ bitlines and ~~a~~ complementary ~~bitline~~ bitlines;

providing a flipped core cell that has ~~a~~ flipped ~~bitline~~ bitlines and ~~a~~ flipped complementary ~~bitline~~ bitlines; and

arranging a plurality of the core cell in a column and a plurality of the flipped core cell in the column, such that the plurality of the core cell equals the plurality of the flipped core cell.

13. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 12, wherein the plurality of the core cell and the plurality of the flipped core cell are aligned in the column that corresponds to the multiple pairs of the global bitline and the global complementary bitline.

14. (original) A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 12, wherein a memory generator is used for designing the memory device.